Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An automatic circuit design apparatus comprising:

a setting module configured to set an upper limit electric potential of a virtual ground line in a circuit to be designed, by use of a cell library for low-threshold cells, a cell library for high-threshold cells, and information of the circuit to be designed; and

a layout generator configured to generate a layout **such that an electric potential of the virtual ground line does not exceed the upper limit electric potential, the layout generated** based on the information, the cell library for low-threshold cells, and the cell library for high-threshold cells.

2. (Original) The automatic circuit design apparatus of claim 1, further comprising a cell library generator configured to generate the cell library for low-threshold cells by using the upper limit electric potential.

3. (Original) The automatic circuit design apparatus of claim 2, wherein the cell library generator comprises:

a delay time calculator configured to calculate delay times of the low-threshold cells; and

a low-threshold cell library generator configured to generate the cell library for low-threshold cells based on the delay times.

4. (Original) The automatic circuit design apparatus of claim 1, wherein the setting module comprises:

a data acquisition module configured to acquire the information, the upper limit electric potential, and a timing constraint; and

an upper limit setting module configured to set an electric potential of a ground terminal in the low-threshold cell to the upper limit electric potential.

5. (Currently Amended) ~~The automatic circuit design apparatus of claim 1,~~ **An automatic circuit design apparatus comprising:**

a setting module configured to set an upper limit electric potential of a virtual ground line in a circuit to be designed, by use of a cell library for low-threshold cells, a cell library for high-threshold cells, and information of the circuit to be designed; and

a layout generator configured to generate a layout based on the information, the cell library for low-threshold cells, and the cell library for high-threshold cells;

wherein the setting module comprises:

a data acquisition module configured to acquire the information, a timing constraint, and a wiring parameter;

a timing constraint determination module configured to calculate an allowable delay time of each cell by estimating the number of high-threshold cells and low-threshold cells based on the information;

an on-resistance calculator configured to calculate an on-resistance of switch cells, based on a transistor characteristic and the cell library for high-threshold cells;

a discharge time calculator configured to calculate the delay time of the low-threshold cells from the discharge time by calculating a discharge time of the low-threshold cells based on the wiring parameter and the on-resistance;

an upper limit calculator configured to calculate the upper limit electric potential by comparing the allowable delay time with the delay time; and

an upper limit setting module configured to set an electric potential of a ground terminal in the low-threshold cell to the upper limit electric potential.

6. (Original) The automatic circuit design apparatus of claim 1, further comprising a logic synthesis module configured to provide a logic synthesis to the information, and to generate a net list.

7. (Currently Amended) ~~The automatic circuit design apparatus of claim 6,~~ **An automatic circuit design apparatus comprising:**

a setting module configured to set an upper limit electric potential of a virtual ground line in a circuit to be designed, by use of a cell library for low-threshold cells, a cell

library for high-threshold cells, and information of the circuit to be designed;

a layout generator configured to generate a layout based on the information, the cell library for low-threshold cells, and the cell library for high-threshold cells; and

a logic synthesis module configured to provide a logic synthesis to the information, and to generate a net list;

wherein the layout generator comprises:

a placement module configured to place the high threshold cells and the low-threshold cells in the net list, based on the cell library for low-threshold cells, the cell library for high-threshold cells, and a timing constraint, and to generate placement data;

a routing module configured to provide a routing process to the placement data, and to generate the layout; and

a switch cell optimizer configured to optimize the arrangement of switch cells to be connected to the virtual ground line when an electric potential of the virtual ground line exceeds the upper limit electric potential.

8. (Original) The automatic circuit design apparatus of claim 7, wherein the placement module comprises:

a high-threshold cell placement module configured to place flip-flops and the high-threshold cells based on the net list;

a low-threshold cell placement module configured to refer to the timing constraint, and to replace the high-threshold cells failing to satisfy the timing constraint with the low-threshold cells;

a switch cell placement module configured to place the switch cell between the virtual ground line and a ground; and

a resistance minimizer configured to shorten a distance between the switch cell and low-threshold cells, connected to common virtual ground line.

9. (Original) The automatic circuit design apparatus of claim 7, wherein the routing module comprises:

a clock routing module configured to route a clock path to the flip-flops;

a general routing module configured to route paths to the high-threshold cells, the

low-threshold cells, and the switch cells; and

a virtual ground line optimizer configured to change a connection of a virtual ground line connected to same-stage low-threshold cells to a connection to other-stage low-threshold cells.

10. (Original) The automatic circuit design apparatus of claim 1, further comprising a circuit modification module configured to add some cells to a net list or remove some cells from the net list in accordance with a timing analysis.

11. (Original) The automatic circuit design apparatus of claim 1, further comprising a timing analyzer configured to provide a timing analysis to the layout based on the cell library for low-threshold cells, the cell library for high-threshold cells, and a timing constraint.

12. (Original) The automatic circuit design apparatus of claim 11, further comprising a modification determination module configured to determine whether there is need to modify a part of the layout in accordance with the timing analysis.

13. (Currently Amended) A method for automatically designing a circuit comprising:

setting an upper limit electric potential of a virtual ground line in a circuit to be designed, by use of a cell library for low-threshold cells, a cell library for high-threshold cells, and information of the circuit to be designed; and

generating a layout **such that an electric potential of the virtual ground line does not exceed the upper limit electric potential, the layout generated** based on the information, the cell library for low-threshold cells, and the cell library for high-threshold cells.

14. (Original) The method of claim 13, further comprising generating the cell library for low-threshold cells by using the upper limit electric potential.

15. (Original) The method of claim 13, further comprising providing a logic synthesis to the information, and generating a net list.

16. (Currently Amended) ~~The method of claim 15,~~ **A method for automatically designing a circuit comprising:**

setting an upper limit electric potential of a virtual ground line in a circuit to be designed, by use of a cell library for low-threshold cells, a cell library for high-threshold cells, and information of the circuit to be designed;

generating a layout based on the information, the cell library for low-threshold cells, and the cell library for high-threshold cells; and

providing a logic synthesis to the information, and generating a net list;

wherein the generation of the layout comprises:

placing the high threshold cells and the low-threshold cells in the net list, based on the cell library for low-threshold cells, the cell library for high-threshold cells, and a timing constraint, and generating a placement data;

routing by the placement data so as to generate the layout; and

optimizing the arrangement of switch cells to be connected to the virtual ground line when an electric potential of the virtual ground line exceeds the upper limit electric potential.

17. (Original) The method of claim 13, wherein the generation of the cell library comprises: calculating delay times of the low-threshold cells; and
generating the cell library for low-threshold cells based on the delay time.

18. (Currently Amended) ~~The method of claim 13,~~ **A method for automatically designing a circuit comprising:**

setting an upper limit electric potential of a virtual ground line in a circuit to be designed, by use of a cell library for low-threshold cells, a cell library for high-threshold cells, and information of the circuit to be designed; and

generating a layout based on the information, the cell library for low-threshold cells, and the cell library for high-threshold cells;

wherein the setting of the upper limit electric potential comprises:

acquiring the information, a timing constraint, and a wiring parameter;

calculating an allowable delay time of each cell by estimating the number of high-threshold cells and low-threshold cells based on the information;

calculating an on-resistance of switch cells, based on a transistor characteristic and the cell library for high-threshold cells;

calculating the delay time of the low-threshold cells from the discharge time by calculating a discharge time of the low-threshold cells based on the wiring parameter and the on-resistance;

calculating the upper limit electric potential by comparing the allowable delay time with the delay time; and

setting an electric potential of a ground terminal in the low-threshold cell to the upper limit electric potential.

19. (Original) The method of claim 1, further comprising providing a timing analysis to the layout based on the cell library for low-threshold cells, the cell library for high-threshold cells, and a timing constraint.

20. (Currently Amended) A computer program product for executing an application for an automatic circuit design apparatus, the computer program product comprising:

instructions configured to set an upper limit electric potential of a virtual ground line in a circuit to be designed, by use of a cell library for low-threshold cells, a cell library for high-threshold cells, and information of the circuit to be designed; and

instructions configured to generate a layout **such that an electric potential of the virtual ground line does not exceed the upper limit electric potential, the layout generated** based on the information, the cell library for low-threshold cells, and the cell library for high-threshold cells.